UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/966,889 | 09/28/2001 | Robert A. Lester | COMP:0234 P01-3624 | 4331 |

7590 11/22/2005

Intellectual Property Administration
Legal Department, M/S 35
PO Box 272400
Ft. Collins, CO 80527-2400

| EXAMINER | |
|---|---|
| CLEARY, THOMAS J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2111 | |

DATE MAILED: 11/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/966,889 | LESTER ET AL. | |
| | Examiner | Art Unit | |
| | Thomas J. Cleary | 2111 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 6, 12, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 5,802,269 to Poisner et al. ("Poisner"), US Patent Number 6,272,601 to Nunez et al. ("Nunez"), and US Patent Number 5,225,085 to Spence ("Spence").

4. In reference to Claim 1, Poisner teaches a system comprising: a processor (See Figure 2 Number 31); a main memory operably coupled to the processor (See Figure 2 Number 35); a cache memory operably coupled to the processor (See Figure 2 Number

39); and a bridge, which is equivalent to a host controller, coupled between the processor and the main memory (See Figure 2 Number 33); the host controller comprising: a memory controller operably coupled to the main memory (See Column 3 Lines 61-63); a processor controller operably coupled to the processor (See Column 3 Lines 64-67); and a coherency controller operably coupled to the cache memory (See Column 3 Lines 61-63). Poisner further teaches that the bridge facilitates communications between the processor, the main memory, and the cache memory (See Column 3 Lines 59-67), and thus it inherently includes an internal bus structure configured to couple each of the memory controller, the processor controller, and the coherency controller to each other. Poisner further teaches sending transactions across the bridge (See Column 3 Lines 64-67), wherein said transactions would inherently be sent in an order, and thus the transactions are ordered transactions. Poisner does not teach that the ordered transactions each have a unique signal type, and wherein each of the individual buses comprises a unidirectional bus configured to transmit only one signal type associated with the request but not including transmission of the data associated with the request. Nunez teaches the use of an interconnect comprised of unidirectional buses (See Column 8 Lines 1-2). Spence teaches a bus interconnect, for transmitting a request of ordered transactions each having a unique signal type, comprising a plurality of individual buses each configured to transmit only one signal type associated with a request but not including transmission of the data associated with the request (See Column 17 Line 60 – Column 18 Line 20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner with the unidirectional interconnect buses of Nunez and the individual buses each carrying a unique non-data signal type of Spence, resulting in the invention of Claim 1, in order to improve performance by eliminating the need for buffers and tri-state drivers typically associated with bi-directional buses (See Column 8 Lines 1-4 of Nunez) and to implement a simple interlocked handshake protocol to transfer data between the components (See Column 17 Lines 60-66 of Spence).

5. In reference to Claim 6, Poisner, Nunez, and Spence teach the limitations as applied to Claim 1 above. Spence further teaches that each signal type corresponds to a single transaction in the particular request operation (See Column 17 Lines 60-62).

6. In reference to Claim 12, Poisner teaches a bridge containing first and second controllers that communicate with each other and thus inherently has an internal bus structure comprising a plurality of individual buses (See Column 3 Lines 59-67). Poisner further teaches sending transactions across the bridge (See Column 3 Lines 64-67), wherein said transactions would inherently be sent in an order, and thus the transactions are ordered transactions. Poisner does not teach that the ordered transactions each have a unique signal type, and each of the individual buses comprising a unidirectional bus configured to transmit only one signal type associated with the request but not including transmission of data associated with the request.

Nunez teaches the use of an interconnect comprised of unidirectional buses (See Column 8 Lines 1-2). Spence teaches a bus interconnect, for transmitting a request of ordered transactions each having a unique signal type, comprising a plurality of individual buses each configured to transmit only one signal type associated with a request but not including transmission of the data associated with the request (See Column 17 Line 60 – Column 18 Line 20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner with the unidirectional interconnect buses of Nunez and the individual buses each carrying a unique non-data signal type of Spence, resulting in the invention of Claim 12, in order to improve performance by eliminating the need for buffers and tri-state drivers typically associated with bi-directional buses (See Column 8 Lines 1-4 of Nunez) and to implement a simple interlocked handshake protocol to transfer data between the components (See Column 17 Lines 60-66 of Spence).

7. In reference to Claim 16, Poisner, Nunez, and Spence teach the limitations as applied to Claim 12 above. Spence further teaches that each signal type corresponds to a single transaction in the particular request operation (See Column 17 Lines 60-62).

8. Claims 2, 3, 4, 5, 13, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner, Nunez, and Spence as applied to Claims 1 and 12 above,

and further in view of US Patent Application Publication Number 2002/0073261 to Kosaraju ("Kosaraju").

9. In reference to Claim 2, Poisner, Nunez, and Spence teach the limitations as applied to Claim 1 above. Poisner; Nunez, and Spence do not teach that the plurality of individual busses is coupled only between two of the memory controller, the processor controller, and the coherency controller. Kosaraju teaches connecting devices together using a point-to-point bus in which each device is connected to only one other device (See Page 2 Paragraph 24).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Poisner, Nunez, and Spence using the point-to-point bus architecture of Kosaraju, resulting in the invention of Claim 2, in order to provide an uninterrupted connection between the two devices and provide a higher bandwidth connection between the two devices (See Page 1 Paragraph 3 of Kosaraju).

10. In reference to Claim 3, Poisner, Nunez, Spence, and Kosaraju teach the limitations as in Claim 2 above. Poisner further teaches that the bridge facilitates communications between the processor and the main memory, (See Column 3 Lines 59-67), and thus it inherently includes the plurality of individual buses coupled between the memory controller and the processor controller.

11. In reference to Claim 4, Poisner, Nunez, Spence, and Kosaraju teach the limitations as in Claim 2 above. Poisner further teaches that the bridge facilitates communications between the cache memory and the main memory, (See Column 3 Lines 59-67), and thus it inherently includes the plurality of individual buses coupled between the memory controller and the coherency controller.

12. In reference to Claim 5, Poisner, Nunez, Spence, and Kosaraju teach the limitations as in Claim 2 above. Poisner further teaches that the bridge facilitates communications between the processor and the cache memory, (See Column 3 Lines 59-67), and thus it inherently includes the plurality of individual buses coupled between the processor controller and the coherency controller.

13. In reference to Claim 13, Poisner, Nunez, and Spence teach the limitations as applied to Claim 12 above. Poisner and Nunez do not teach that each individual bus is coupled between only a first controller and a second controller. Kosaraju teaches connecting devices together using a point-to-point bus in which each device is connected to only one other device (See Page 2 Paragraph 24).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Poisner, Nunez, and Spence using the point-to-point bus architecture of Kosaraju, resulting in the invention of Claim 13, in order to provide an uninterrupted connection between the two devices and provide a

higher bandwidth connection between the two devices (See Page 1 Paragraph 3 of Kosaraju).

14. In reference to Claim 14, Poisner, Nunez, Spence, and Kosaraju teach the limitations as applied to Claim 13 above. Poisner further teaches that the first controller comprises a processor controller (See Column 3 Lines 64-67).

15. In reference to Claim 15, Poisner, Nunez, Spence, and Kosaraju teach the limitations as applied to Claim 13 above. Poisner further teaches that the second controller comprises a memory controller (See Column 3 Lines 61-63).

16. Claims 7, 8, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner, Nunez, and Spence as applied to Claims 6 and 16 above, and further in view of US Patent Number 6,584, 031 to Hanaoka et al. ("Hanaoka").

17. In reference to Claim 7, Poisner, Nunez, and Spence teach the limitations as applied to Claim 6 above. Poisner, Nunez, and Spence do not teach that each respective signal type includes an identification tag. Hanaoka teaches the use of a header that provides an identification tag for data communicated across a serial interface (See Figure 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner, Nunez, and Spence with the

header of Hanaoka, resulting in the invention of Claim 18, in order allow the data to be sent in a well-known packet format that can provide information to the receiver regarding the data as well as provide a cyclic redundancy check of the data to insure proper receipt (See Figure 4 of Hanaoka).

18. In reference to Claim 8, Poisner, Nunez, Spence, and Hanaoka teach the limitations as applied to Claim 7 above. Hanaoka further teaches that the identification tag comprises a source identification, a destination identification, and a priority identification, which is equivalent to a cycle identification (See Figure 4).

19. In reference to Claim 17, Poisner, Nunez, and Spence teach the limitations as applied to Claim 16 above. Poisner, Nunez, and Spence do not teach that each signal type includes an identification tag. Hanaoka teaches the use of a header that provides an identification tag for data communicated across a serial interface (See Figure 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner, Nunez, and Spence with the header of Hanaoka, resulting in the invention of Claim 18, in order allow the data to be sent in a well-known packet format that can provide information to the receiver regarding the data as well as provide a cyclic redundancy check of the data to insure proper receipt (See Figure 4 of Hanaoka).

20. In reference to Claim 18, Poisner, Nunez, Spence, and Hanaoka teach the limitations as applied to Claim 17 above. Hanaoka further teaches that the identification tag comprises a source identification, a destination identification, and a priority identification, which is equivalent to a cycle identification (See Figure 4).

21. Claims 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner, Nunez, Spence, and Hanaoka as applied to Claims 8 and 18 above, and further in view of US Patent Number 6,130,886 to Ketseoglou et al. ("Ketseoglou").

22. In reference to Claim 9, Poisner, Nunez, Spence, and Hanaoka teach the limitations as applied to Claim 8 above. Poisner, Nunez, Spence, and Hanaoka do not teach that the cycle identification comprises a toggle bit configured to free the cycle identification for re-use before each transaction in the request operation is complete. Ketseoglou teaches a correlative ID field that appears in signal messages until the link is dropped and can be changed during a connection, and thus enables reuse of the identification before the operation is complete (See Column 11 Lines 60-62 and Column 13 Lines 57-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner, Nunez, Spence, and Hanaoka with the reusable identification numbers of Ketseoglou, resulting in the invention of Claim 9, in order to allow reuse of the identification number before the connection is completed (See Column 13 Lines 56-61 of Ketseoglou).

23. In reference to Claim 19, Poisner, Nunez, Spence, and Hanaoka teach the limitations as applied to Claim 18 above. Poisner, Nunez, Spence, and Hanaoka do not teach that the cycle identification comprises a toggle bit configured to free the cycle identification for re-use before each transaction in the request operation is complete. Ketseoglou teaches a correlative ID field that appears in signal messages until the link is dropped and can be changed during a connection, and thus enables reuse of the identification before the operation is complete (See Column 11 Lines 60-62 and Column 13 Lines 57-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner, Nunez, Spence, and Hanaoka with the reusable identification numbers of Ketseoglou, resulting in the invention of Claim 19, in order to allow reuse of the identification number before the connection is completed (See Column 13 Lines 56-61 of Ketseoglou).

24. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner, Nunez, and Spence as applied to Claim 1 above, and further in view of US Patent Number 5,901,281 to Miyao et al. ("Miyao").

25. In reference to Claim 10, Poisner, Nunez, and Spence teach the limitations as applied to Claim 1 above. Poisner, Nunez, and Spence do not teach that the processor

comprises the cache memory. Miyao teaches using a processor that has an internal cache (See Column 3 Lines 24-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Poisner, Nunez, and Spence with the processor internal cache of Miyao, resulting in the invention of Claim 10, because recent microprocessors generally contain internal cache memories because of improved integration (See Column 3 Lines 24-27 of Miyao).

26. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner, Nunez, and Spence as applied to Claim 1 above, and further in view of US Patent Number 6,587,930 to Deshpande et al. ("Deshpande").

27. In reference to Claim 11, Poisner, Nunez, and Spence teach the limitations as applied to Claim 1 above. Poisner, Nunez, and Spence do not teach a plurality of processor buses; a plurality of processing units, wherein each processing unit is coupled to a respective one of the plurality of processor buses; and a plurality of processor controllers, each processor controller corresponding to a respective one of the plurality of processor buses, wherein the processor controllers are not directly coupled to each other via the internal bus structure. Deshpande teaches a plurality of processor buses (See Figure 4 Numbers 413 and 414); a plurality of processing units, wherein each processing unit is coupled to a respective one of the plurality of processor buses (See Figure 4 Numbers 411 and 412); a plurality of processor controllers, each

processor controller corresponding to a respective one of the plurality of processor buses (See Figure 6), and wherein the processor controllers are not directly coupled to each other via the internal bus structure (See Figure 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner, Nunez, and Spence with the plurality of processing units, processing buses, and processing controllers of Deshpande, resulting in the invention of Claim 11, in order to increase the speed and reliability of the system by utilizing multiple processors as well as to help maintain cache coherency by preventing read-read deadlocks (See Abstract of Deshpande).

***Drawings***

28. The drawings are objected to because Numbers 16 and 18 of Figure 1 have been reversed and are inconsistent with the elements identified as Numbers 16 and 18 in the Specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the

drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

29. Applicant has stated that a replacement drawing sheet of Figure 1 was submitted as Appendix A to correct the reversal of element numbers 16 and 18 in the replacement sheet of Figure 1 submitted on 23 December 2004. A copy of Appendix A is not currently present in the application file. The Applicant is requested to resubmit the replacement drawing sheet of Figure 1 (Appendix A) in order to make it of record in the application file.

***Response to Arguments***

30. Applicant has stated that "the internal data bus, when viewed in light of the specification, is not configured to transmit data signals" (See Page 7 Paragraph 2 Lines 8-9). Applicant has further stated that "the requested data is transmitted through the data controller via a data bus" (See Page 8 Paragraph 1 Lines 8-9). It is unclear how data is transmitted via a data bus if the data bus is not configured to transmit data signals.

31. Applicant has stated that "the disclosed and recited internal bus structure is configured to send the ordered exchanges or transactions associated with a particular request" and "the data associated with a particular request is not sent along the internal bus structure, but rather is sent on a data bus" (See Page 8 Paragraph 2 – Page 9 Paragraph 2). Accordingly, the Examiner will interpret the internal bus structure of the host controller to be configured to send only the ordered exchanges or transactions associated with a request, and not the data associated with the request, which is exchanged on a data bus through a data controller under the direction of the host controller.

32. Applicant's arguments, see Pages 6-17, filed 4 November 2005, with respect to the rejection(s) of Claim(s) 1-19 under 35 U.S.C. §§ 103 and 112 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art.

***Conclusion***

33. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3), Alt. Fridays (7-2).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
11/16/05

Thomas J. Cleary
Patent Examiner
Art Unit 2111